Sonoma State University  
Department of Engineering Science 

EE 330 Electronics II  
Fall 2017 

Units: 2.0 

Schedule/Location: M, 09:00–11:50; W, 11:00–11:50 / Salazar 2005 

Instructor: Mohamed Salem  
Office: Salazar 2010B  
Phone: (707) 664-3543  
Email: mohamed.salem@sonoma.edu (Please add [EE330] to email subject)  
Hours: MT, 12:00–14:00; R, 16:00–17:00 (drop by/email) 

Description: Analysis and design of high frequency amplifiers; high frequency models of transistors; operational amplifiers and applications; feedback amplifiers; oscillators, modulators, bandpass amplifiers, and demodulators for communications. Laboratory work. 

Prerequisites: EE 230. 


Web: https://moodle.sonoma.edu/C/
Course Policies

Homework:

- Approximately one homework assignment every week with total points scaled to 10.
- Homework is due at the beginning of session one week after its assignment.
- Late assignments will be awarded up to 5 points if received within five days of due date.
- Assignments must be completed neatly in pen or pencil, preferably on engineering paper.

Quizzes:

- Quizzes may be given at instructor’s discretion and cannot be made up.
- Quizzes are added to homework grade.

Exams:

- Two mid-term exams scheduled after completing Chapter 7, and after completing Chapter 8.
- Total points for each exam are scaled to 100.
- One comprehensive final exam scheduled between 09:00-11:50 on Monday, Dec. 11, 2017.
- Total points for the final exam are scaled to 200.
- No exam may be taken outside scheduled time without prior arrangement with instructor.
- No exams can be made up if student does not show up at the scheduled or arranged time.
- No electronic devices other than an approved calculator may be used while taking any exams.

Labs:

- Students must prepare the experiment before the lab session.
- Formal laboratory report is required one week after the completion of the experiment.
- Total points for each report are scaled to 100.
- Late reports will be awarded up to 60 points if received within five days of due date.

Assessment and Grading:

- No late work will be accepted after 17:00, Wednesday, Dec. 06, 2017.
- It is the student’s responsibility to communicate late submission with instructor.
- Illegible, stained, or scribbled on assignments may receive partial or no credit.
- Final grade is based on the weighting shown below

<p>| | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Homework:</td>
<td>25%</td>
</tr>
<tr>
<td>Lab reports:</td>
<td>25%</td>
</tr>
<tr>
<td>Mid-term exams:</td>
<td>25%</td>
</tr>
<tr>
<td>Final exam:</td>
<td>25%</td>
</tr>
</tbody>
</table>

Grade scale that will be used for total percentage points and corresponding letter grade are given below

<table>
<thead>
<tr>
<th></th>
<th>0</th>
<th>60</th>
<th>63</th>
<th>67</th>
<th>70</th>
<th>73</th>
<th>77</th>
<th>80</th>
<th>83</th>
<th>87</th>
<th>90</th>
<th>95</th>
<th>100</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>F</td>
<td>D-</td>
<td>D</td>
<td>D+</td>
<td>C-</td>
<td>C</td>
<td>C+</td>
<td>B-</td>
<td>B</td>
<td>B+</td>
<td>A-</td>
<td>A</td>
<td></td>
</tr>
</tbody>
</table>

EE 330 Electronics II 2/6 Sonoma State University
Academic Integrity

You are responsible to behave ethically and honestly. Copying, cheating, forgery, and other unethical or dishonest actions are not tolerated, will result in a zero grade, and may be reported to SSU authorities. For more information on SSU policy on academic cheating and plagiarism please refer to: http://www.sonoma.edu/uaffairs/policies/cheating_plagiarism.htm

Classroom Learning Civility Clause

In any environment in which people gather to learn, it is essential that all members feel as free and safe as possible in their participation. To this end, it is expected that everyone in this course will be treated with mutual respect and civility, with an understanding that all of us (students, instructors, professors, guests, and teaching assistants) will be respectful and civil to one another in discussion, in action, in teaching, and in learning.

Should you feel our classroom interactions do not reflect an environment of civility and respect, you are encouraged to meet with your instructor during office hours to discuss your concern. For additional information and resources, please refer to SSU policy on civility and tolerance at: http://www.sonoma.edu/students/civility_tolerance.pdf

Disability Support Services

Reasonable accommodations are available for students who have documented temporary or permanent disabilities. All accommodations must be approved through Disability Support Services located in Salazar Hall, Room 1049 in order to notify your instructor(s) as soon as possible regarding accommodation(s) needed for the course.

- Phone: (707) 664-2677
- Email: disability.services@sonoma.edu
- Web: http://www.sonoma.edu/dss/students/dss_services.html

For more information on SSU policy on disability access for students, please refer to: http://www.sonoma.edu/uaffairs/policies/disabilitypolicy.htm

Other Policies

Be sure you understand the policies that specifically affect you as a student of this course, such as:

- Add/Drop Policy: http://www.sonoma.edu/catalog/08-10/17regulations.pdf#adddrop
- Grade Appeal Policy: http://www.sonoma.edu/uaffairs/policies/grade_appeal.htm
Course Learning Objectives (CLOs)

By the end of this course, the student should be able to:

A. apply fundamental device and circuit design concepts to a variety of analog semiconductor electronic circuits
B. apply core operational principles of semiconductor devices to electronic circuit analysis and design
C. demonstrate an ability to design and make measurements on analog electronic circuits and write formal laboratory reports
D. develop critical thinking skills through electronic circuit analysis and design

Student Learning Outcome vs Course Learning Objectives

<table>
<thead>
<tr>
<th>ABET Students Outcomes</th>
<th>CLOs</th>
<th>Level of Support</th>
</tr>
</thead>
<tbody>
<tr>
<td>(a) an ability to apply knowledge of mathematics, science, and engineering</td>
<td>A, B, D</td>
<td>4</td>
</tr>
<tr>
<td>(b) an ability to design and conduct experiments, as well as to analyze and interpret data</td>
<td>C</td>
<td>3</td>
</tr>
<tr>
<td>(c) an ability to design a system, component, or process to meet desired needs</td>
<td>A-D</td>
<td>3</td>
</tr>
<tr>
<td>(d) an ability to function on multi-disciplinary teams</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(e) an ability to identify, formulate, and solve engineering problems</td>
<td>A, B, D</td>
<td>3</td>
</tr>
<tr>
<td>(f) an understanding of professional and ethical responsibility</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(g) an ability to communicate effectively</td>
<td>C</td>
<td>2</td>
</tr>
<tr>
<td>(h) the broad education necessary to understand the impact of engineering solutions in a global and societal context</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(i) a recognition of the need for, and an ability to engage in life-long learning</td>
<td>D</td>
<td>2</td>
</tr>
<tr>
<td>(j) a knowledge of contemporary issues</td>
<td></td>
<td>0</td>
</tr>
<tr>
<td>(k) an ability to use the techniques, skills, and modern engineering tools necessary for engineering practice</td>
<td>C</td>
<td>2</td>
</tr>
</tbody>
</table>

Level of support (0-5): 0=No support, 1=Lowest support, 5=Highest support

Assessment Methods

Assessment of student learning:

1. Examination (mid-term and final exams)
2. Homework assignments
3. Lab reports

Assessment of course quality:

1. Student survey
2. Student verbal and peer instructor feedback
<table>
<thead>
<tr>
<th>Week</th>
<th>Monday</th>
<th>Wednesday</th>
</tr>
</thead>
<tbody>
<tr>
<td>1. 08/21 &amp; 08/23</td>
<td>No Class</td>
<td>Introduction / Bipolar Junction Transistors Syllabus. BJT structure and physical operation</td>
</tr>
<tr>
<td>2. 08/28 &amp; 08/30</td>
<td>Bipolar Junction Transistors (Ch. 6) I-V characteristics</td>
<td>Bipolar Junction Transistors Circuits at DC, breakdown and temperature effects</td>
</tr>
<tr>
<td>3. 09/04 &amp; 09/06</td>
<td>Labor Day – No Class</td>
<td>Transistor Amplifiers (Ch. 7) Voltage gain, biasing, Q point</td>
</tr>
<tr>
<td>4. 09/11 &amp; 09/13</td>
<td>Transistor Amplifiers Small signal model, MOSFET vs BJT</td>
<td>Transistor Amplifiers Basic configurations</td>
</tr>
<tr>
<td>5. 09/18 &amp; 09/20</td>
<td>Transistor Amplifiers Basic configurations, general rules</td>
<td>Transistor Amplifiers Discrete circuits, bode plots</td>
</tr>
<tr>
<td>6. 09/25 &amp; 09/27</td>
<td>Transistor Amplifiers Bode plots, frequency response</td>
<td>Transistor Amplifiers frequency response, review</td>
</tr>
<tr>
<td>7. 10/02 &amp; 10/04</td>
<td>Mid-term exam 1</td>
<td>Building Blocks of IC Amplifiers (Ch. 8) IC biasing</td>
</tr>
<tr>
<td>8. 10/09 &amp; 10/11</td>
<td>Building Blocks of IC Amplifiers Basic gain cell</td>
<td>Building Blocks of IC Amplifiers Basic gain cell</td>
</tr>
<tr>
<td>9. 10/16 &amp; 10/18</td>
<td>Building Blocks of IC Amplifiers Common-gate, common-base, cascade</td>
<td>Building Blocks of IC Amplifiers Common-gate, common-base, cascade</td>
</tr>
<tr>
<td>10. 10/23 &amp; 10/25</td>
<td>Building Blocks of IC Amplifiers Different configurations</td>
<td>Building Blocks of IC Amplifiers Current mirrors and scaling</td>
</tr>
<tr>
<td>11. 10/30 &amp; 11/01</td>
<td>Mid-term Exam 2</td>
<td>Differential and Multistage Amplifiers (Ch. 9) MOS and BJT differential pairs</td>
</tr>
<tr>
<td>12. 11/06 &amp; 11/08</td>
<td>Differential and Multistage Amplifiers MOS and BJT differential pairs</td>
<td>Differential and Multistage Amplifiers Common mode rejection</td>
</tr>
<tr>
<td>13. 11/13 &amp; 11/15</td>
<td>Differential and Multistage Amplifiers Current mirror load</td>
<td>Differential and Multistage Amplifiers Current mirror load</td>
</tr>
<tr>
<td>14. 11/20 &amp; 11/22</td>
<td>Differential and Multistage Amplifiers Multistage amplifiers</td>
<td>Thanksgiving – No Class</td>
</tr>
<tr>
<td>15. 11/27 &amp; 11/29</td>
<td>Frequency Response (Ch. 10) Low-frequency response</td>
<td>Frequency Response Low-frequency response, internal capacitance</td>
</tr>
<tr>
<td>16. 12/04 &amp; 12/06</td>
<td>Frequency Response Internal capacitance, high-frequency response</td>
<td>Frequency Response High-frequency response</td>
</tr>
<tr>
<td>17. 12/11</td>
<td></td>
<td>Final Exam</td>
</tr>
</tbody>
</table>
### Lab Schedule

<table>
<thead>
<tr>
<th>Date</th>
<th>Topic</th>
</tr>
</thead>
<tbody>
<tr>
<td>08/21</td>
<td>No Lab</td>
</tr>
<tr>
<td>08/28</td>
<td>No Lab</td>
</tr>
<tr>
<td>09/04</td>
<td>Labor Day – No Class</td>
</tr>
<tr>
<td>09/11</td>
<td>NPN and PNP I-V Characteristics</td>
</tr>
<tr>
<td>09/18</td>
<td>NPN and PNP at DC</td>
</tr>
<tr>
<td>09/25</td>
<td>NPN Common-Emitter Amplifier</td>
</tr>
<tr>
<td>10/02</td>
<td>NMOS Common-Source Amplifier</td>
</tr>
<tr>
<td>10/09</td>
<td>NPN Emitter-Follower</td>
</tr>
<tr>
<td>10/16</td>
<td>BJT Current Mirror</td>
</tr>
<tr>
<td>10/23</td>
<td>Bipolar Differential Amplifier</td>
</tr>
<tr>
<td>10/30</td>
<td>Bipolar Phase Shift Oscillator</td>
</tr>
<tr>
<td>11/06</td>
<td>Project</td>
</tr>
<tr>
<td>11/13</td>
<td>Project</td>
</tr>
<tr>
<td>11/20</td>
<td>Project</td>
</tr>
<tr>
<td>11/27</td>
<td>Project Presentation</td>
</tr>
<tr>
<td>12/04</td>
<td>Makeup Lab</td>
</tr>
</tbody>
</table>

Note: schedules are subject to change.