Problem 1 (14 points)
Design a MOS differential amplifier (DA) illustrated in the schematic below to operate at overvoltage $V_{OV} = 0.25$ volt with a transconductance $g_m = 1$ mA/V. Find the $(W/L)$ ratio and the bias current tail current $I$ meeting these requirements. The process technology used to construct the NMOS devices have parameters values of $V_t = 0.5$ volt and $\mu n C_{OX} = 0.4$ mA/V$^2$. Assume the two devices are identical and ignore the drain-to-source resistance $r_d$.

\[ I = \ldots \text{mA} \]

\[(W/L) = \ldots\]
Problem 2 (21 points)
Design a MOS differential amplifier (DA) to operate from power supply voltages of $V_{DD} = 1\, \text{V}$ and $V_{SS} = -1\, \text{V}$, and dissipating at most 1 mW of power $P$ at its quiescent state (i.e., no applied input signal). Find the value of $V_{OV}$ so that a value for the differential input voltage, namely, $V_{id} = 0.25\, \text{V}$, steers all current to one device (i.e., no current to the other device – one device on and other off). The magnitude of the differential voltage gain $A_{\text{diff}}$ is to be 10 V/V. Assume device parameters of $\mu_n C_{\text{OX}} = 0.4\, \text{mA/V}^2$ and neglect the Early effect (i.e., ignore $r_0$). Find tail current $I$, the drain load resistor $R_D$ and the device gate width-to-length ($W/L$) ratio.

$I = \underline{\text{ ______ } \text{mA}}$

$R_D = \underline{\text{ ______ } \text{k}\Omega}$

$(W/L) = \underline{\text{ ______ }}$
Problem 3 (21 points)

(a) Draw the AC schematic circuit of the differential half-circuit for the differential amplifier cell shown immediately below. [This makes use of symmetry within a DA.]

(b) Derive an expression for the differential gain $A_d$ (defined as $v_{od}/v_{id}$) as a function of $g_m$, $R_D$ and the bridging resistor $R_S$. Neglect the Early effect (i.e., ignore $r_0$).

(c) What is the differential voltage gain with $R_S = 0$?
(d) What is the value of $R_s$ (express it in terms of $1/g_m$) that reduces the differential gain calculated in part (b) to one-half of that value?

Problem 4 (21 points)
Consider the BJT differential amplifier shown below. Initially assume $\beta$ is very large.

(a) What is the largest input common-mode signal that can be applied while the BJTs remain comfortably within the active region of operation while maintaining $V_{CB} = 0$ volt? Write an expression in terms of $V_{CC}$, tail current $I$ and collector resistance $R_C$.

(b) If the available power supply $V_{CC}$ is 2.0 volts, what is the value of $I \cdot R_C$ that should be chosen to allow a common-mode input signal of $\pm 1$ volt?
(c) Using the $I \cdot R_C$ value you found in part (b), select values for $I$ and $R_C$. Now we assume that the current gain $\beta = 100$. Use the largest possible value for tail current $I$ subject to the constraint that the base current of each transistor (given that $I$ is divided equally between the transistors) should not exceed 2 $\mu$A ($= 0.002$ mA).

Problem 5 (23 points)
Design a BJT differential amplifier (DA) to amplify a differential input signal with an amplitude of 0.1 volt and give a differential output signal amplitude of 2 volts. To ensure adequate linearity, it is required that the signal amplitude across each base-emitter junction not exceed a maximum of 5 millivolts. An additional design requirement is that the differential input resistance be at least 100 k$\Omega$. The BJTs that are used in this differential amplifier have a $\beta = 100$ (how convenient!). Using your circuit configuration specify the component values ($i.e.$, power supply voltage $V_{CC}$ and resistor values). You may use an ideal current source for forcing the tail current ($I_{EE}$) in the differential amplifier. [Hint: You will probably need to use emitter degeneration resistance to meet these requirements.]