Synchronization

EE442 – Lecture 17

All digital receivers must be synchronized to the incoming signal $s(t)$. This means we must have a way to perform

1. **Bit or symbol** synchronization
2. **Frame** synchronization
3. **Carrier and/ or clock** synchronization

http://mwrf.com/markets/regenerate-coherent-carriers-psk-signals
Pulse Restoration or Regeneration Goal

Function of Amplification

Initial Pulse into Channel → Pulse as received → After Amplification

Function of Regeneration

Initial Pulse into Channel → Pulse as received → As Regenerated

Synchronization Overview

Synchronization in a binary receiver:

\[ s(t) \]

\[ \text{LPF} \]

\[ \text{Regenerator} \]

\[ \text{Frame Sync} \]

\[ \text{Frame Indicator} \]

\[ \text{Output Message} \]

\[ \text{Incoming Signal} \]

\[ \text{Bit Sync} \]

\[ \text{Clock} \]

We not only need to recover the data but also the clock (both phase & frequency).

Polar NRZ to Unipolar “Open-Loop” Bit Synchronization

\[
\cos(2\pi R_b t + \phi)
\]

Another “Open-Loop” Bit Synchronization Technique

\[ f_o = R_b \]

\[ \frac{ds(t)}{dt} \] produces both “+” and “-” pulses; squaring the \( \frac{ds}{dt} \) output results in all pulses being “+”. Next we filter with a high-Q BPF centered at the \( f_{\text{clock}} \).

“Closed-Loop” Bit Synchronization – Early/Late Gate Sync (1)

Bit data synchronization by comparative measurements between the incoming sign \( s(t) \) and a locally generated clock signal. This can also be used for carrier tracking.
"Closed-Loop" Bit Synchronization – Early/Late Gate Sync (2)

\[
\begin{align*}
\text{Early Gate Integration} & : & s_1(t) & = T - d \\
\text{Late Gate Integration} & : & s_2(t) & = d + T - d \\
\text{Error} & : & e & = 0
\end{align*}
\]

\[
\begin{align*}
\text{Early Gate Integration} & : & s_1(t) & = T + d \\
\text{Late Gate Integration} & : & s_2(t) & = d - T - d \\
\text{Error} & : & e & = -2\Delta
\end{align*}
\]

No change!

This reduces the frequency of the VCO clock signal.

Requires a data state change before and after the channel bit.
What is a Phase lock Loop?

1. A negative feedback control system whose operation is closely linked to frequency modulation (FM is our next topic)

2. Automatically adjusts the frequency and phase of a controlled oscillator to match a reference (or input) frequency

3. Commonly used for carrier synchronization and indirect frequency demodulation

4. A change in the input signal shows up as a change in phase of the input signal and the VCO frequency
Components in a Phase lock Loop

1. Phase detector (phase difference to voltage output)
2. Voltage-controlled oscillator (VCO)
3. Low-pass filter (filters out HF content of phase detector)

Mathematical expressions:

\[ A[\cos \omega_c t + \theta_i(t)] \]

\[ 2B[\cos \omega_c t + \theta_o(t)] \]

\[ H(s) \]

Lathi & Ding
Pages 212-213
Some Common Applications of a Phase lock Loop

1. Frequency multiplier which multiplies frequency of a reference oscillator
2. Modulator by adding modulating signal to phase error
3. Demodulator which tracks changes in modulation
4. Coherent receiver operating as a narrow band tunable filter to track the carrier frequency
5. Data synchronizer operating as narrow band tunable filter to recover the clock frequency (digital communication systems)
Phase Detector From a XOR Gate

The area under the pulses is proportional to the phase difference $\Delta \phi$. 

<table>
<thead>
<tr>
<th>$X_1$</th>
<th>$X_2$</th>
<th>$X_{out}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>
Low-Pass Filtering PD Output $V_{pd}$

Low Pass Filter

- The output signal of the PD (shown in figure) cannot be directly fed to the VCO.
- We need to feed the VCO with DC voltage signal that corresponds to the phase difference ($\Delta \Phi$).
- Thus, we need a LPF to smoothen the PD output signal (turns it into DC voltage signal) that corresponds to ($\Delta \Phi$).
Low-Pass Filtering PD Output $V_{pd}$

LPF output

- The output voltage from the PD (multiplier) is:
  \[
  \frac{AB}{2} (\cos(\omega t + \omega t + \phi_1 + \phi_2) + \cos(\phi_1 - \phi_2))
  \]

- The LPF will eliminate this term \((\cos(\omega t + \omega t + \phi_1 + \phi_2))\) which represents high frequency.

- The output from the LPF will be \(\cos(\phi_1 - \phi_2)\) which is \((\Delta \Phi)\):
  \[
  \cos(\phi_1 - \phi_2) \approx \phi_1 - \phi_2 = \Delta \phi
  \]
In the case of carrier-recovery in which coherent demodulation is to be performed on QAM-type signals, the **Costas loop** has found wide-spread use as an unbiased low-variance practical solution.
Costas Receiver Uses a Phase Lock Loop

A_{C}m(t) \cdot \cos(2\pi f_{C}t)
Questions?