Setting up the ADC
Analog-to-digital converter (ADC)
Chapter 11 – Ref. Manual

Updated: 4/9/18
Basics

- The 12-bit ADC is a successive approximation analog-to-digital converter.
- It has up to 19 multiplexed channels allowing it to measure signals from 16 external sources, two internal sources, and the VBAT channel.
- The A/D conversion of the channels can be performed in single, continuous, scan or discontinuous mode.
  - Single and continuous conversion modes
  - Scan mode for automatic conversion of channel 0 to channel ‘n’
- The result of the ADC is stored into a left or right-aligned 16-bit data register.
ADC Registers

The converted data are stored into the 16-bit ADC_DR register.

Setting ADC_CR2 register (for a regular channel only)

Find the registers in the ref. manual and read about them!
Channel Selection

- There are 16 multiplexed channels.
- It is possible to organize the conversions in two groups: **regular and injected**.
- A **group** consists of a sequence of conversions that can be done on any channel and in any order. For instance, it is possible to implement the conversion sequence in the following order: `ADC_IN3, ADC_IN8, ADC_IN2, ADC_IN2, ADC_IN0, ADC_IN2, ADC_IN2, ADC_IN15`.

- A **regular group** is composed of up to 16 conversions. The regular channels and their order in the conversion sequence must be selected in the `ADC_SQRx` registers.
  - The total number of conversions in the regular group must be written in the `L[3:0]` bits in the `ADC_SQR1` register.

- An **injected group** is composed of up to 4 conversions. The injected channels and their order in the conversion sequence must be selected in the `ADC_JSQR` register.
  - The conversion is done on one channel in each group at a time.
ADC: Regular vs injected

The diagram illustrates the flow of data and control signals in an ADC system. It shows the connection between GPIO ports, MUX, analog to digital converter (ADC), and data registers.

- **16MHz HSI** is connected to the divider (1, 2, 4) and generates ADC_CLOCK.
- **GPIO Ports** connect to **MUX**, which routes signals to **Up to 4 Injected Channels** or **Up to 16 Regular Channels**.
- **Analog to Digital Converter** processes the signals into **Injected Channels** and **Regular Channels**.
- **Injected Data Register** includes **Injected Data Register 1** to **Injected Data Register 4**.
- **Regular Data Register**
- **DMA Request**, **End of Conversion**, **End of Injected Conversion**, **Overrun**, and **Analog Watchdog Event** are signals that can trigger interrupts.
- **Analog Watchdog** registers track high and low thresholds.

The system uses data and address buses for communication.
AN0 = PA0

Ax IS ANALOG/ Dx IS DIGITAL
ADC Mode

Single Channel, Single Conversion Mode
CONT in ADC_CR2 = 0
SCAN in ADC_CR2 = 0

Single Channel, Continuous Conversion Mode
CONT in ADC_CR2 = 1
SCAN in ADC_CR2 = 0

Scan Mode with Single Conversion
SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 0

Scan Mode with Continuous Conversion
SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 1
ADC Mode

- Channels are selected by ADC_SQRx registers for regular channels, and by ADC_JSQR register for injected channel.

- All channels in a regular group share the same result register ADC_DR. Make sure to read data between consecutive sampling.

---

Scan Mode with Single Conversion
SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 0

Scan Mode with Continuous Conversion
SCAN in ADC_CR2 = 1
CONT in ADC_CR2 = 1
ADC Mode

**Regular channel:**
1. Set SWSTART in ADC_CR2
2. The channel is selected by SQ1[4:0] in SQR5
3. Result is stored in ADC_DR
4. EOC is set after conversion
5. Interrupt is generated if EOCIE is set

**Injected channel:**
1. Set JSWSTART in ADC_CR2
2. The channel is selected by JSQ1[4:0] in JSQR
3. Result is stored in ADC_JDR1
4. JEOC is set after conversion
5. Interrupt is generated if JEOCIE is set
Data Alignment

Right alignment for a regular channel:
- 6 bits: 00000000
- 8 bits: 000000000
- 10 bits: 0000000000
- 12 bits: 00000000000

Right alignment for an injected channel:
- 6 bits: Sign Ext [9:0]
- 8 bits: Sign Ext [7:0]
- 10 bits: Sign Ext [5:0]
- 12 bits: Sign Ext [3:0]

Left alignment for a regular channel:
- 6 bits: 00000000
- 8 bits: XXXXXXXX 00000000
- 10 bits: XXXXXXXX 000000
- 12 bits: XXXXXXXX 00000

Left alignment for an injected channel:
- 6 bits: Sign Ext [8:0]
- 8 bits: S XXXXXXXX 0000000
- 10 bits: S XXXXXXXX 00000
- 12 bits: S XXXXXXXX 000 0

S = Sign bit