Parallel Inputs and Outputs

Four Operating Modes:
- Synchronous Parallel Load
- Right Shift
- Left Shift
- Do Nothing

Positive Edge-Triggered Clocking

Direct Overriding Clear

<table>
<thead>
<tr>
<th>TYPE</th>
<th>MAXIMUM CLOCK FREQUENCY</th>
<th>TYPICAL POWER DISSIPATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>'194</td>
<td>36 MHz</td>
<td>165 mW</td>
</tr>
<tr>
<td>'LS194A</td>
<td>35 MHz</td>
<td>75 mW</td>
</tr>
<tr>
<td>'3194</td>
<td>103 MHz</td>
<td>425 mW</td>
</tr>
</tbody>
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description

These bidirectional shift registers are designed to incorporate virtually all of the features a system designer may want in a shift register. The circuit contains 48 equivalent gates and features parallel inputs, parallel outputs, right-shift and left-shift serial inputs, operating-mode-control inputs, and a direct overriding clear line. The register has four distinct modes of operation, namely:

- Inhibit clock (do nothing)
- Shift right (in the direction QA toward QD)
- Shift left (in the direction QD toward QA)
- Parallel (broadside) load

Synchronous parallel loading is accomplished by applying the four bits of data and taking both mode control inputs, S0 and S1, high. The data are loaded into the associated flip-flops and appear at the outputs after the positive transition of the clock input. During loading, serial data flow is inhibited.

Shift right is accomplished synchronously with the rising edge of the clock pulse when S0 is high and S1 is low. Serial data for this mode is entered at the shift-right data input. When S0 is low and S1 is high, data shifts left synchronously and new data is entered at the shift-left serial input.

Clocking of the shift register is inhibited when both mode control inputs are low. The mode controls of the SN54194/SN74194 should be changed only while the clock input is high.
schematics of inputs and outputs
typical clear, load, right-shift, left-shift, inhibit, and clear sequences