DUAL N-CHANNEL AND DUAL P-CHANNEL MATCHED MOSFET PAIR

GENERAL DESCRIPTION
The ALD1103 is a monolithic dual N-channel and dual P-channel matched transistor pair intended for a broad range of analog applications. These enhancement-mode transistors are manufactured with Advanced Linear Devices' enhanced ACMOS silicon gate CMOS process. It consists of an ALD1101 N-channel MOSFET pair and an ALD1102 P-channel MOSFET pair in one package.

The ALD1103 offers high input impedance and negative current temperature coefficient. The transistor pair is matched for minimum offset voltage and differential thermal response, and it is designed for precision signal switching and amplifying applications in +2V to +12V systems where low input bias current, low input capacitance and fast switching speed are desired. Since these are MOSFET devices, they feature very large (almost infinite) current gain in a low frequency, or near DC, operating environment. When used in pairs, a dual CMOS analog switch can be constructed. In addition, the ALD1103 is intended as a building block for differential amplifier input stages, transmission gates, and multiplexer applications.

The ALD1103 is suitable for use in precision applications which require very high current gain, beta, such as current mirrors and current sources. The high input impedance and the high DC current gain of the Field Effect Transistors result in extremely low current loss through the control gate. The DC current gain is limited by the gate input leakage current, which is specified at 50pA at room temperature. For example, DC beta of the device at a drain current of 5mA at 25°C is 5mA/50pA = 100,000,000.

FEATURES
- Thermal tracking between N-channel and P-channel pairs
- Low threshold voltage of 0.7V for both N-channel & P-channel MOSFETS
- Low input capacitance
- Low Vos -- 10mV
- High input impedance -- 10^12Ω typical
- Low input and output leakage currents
- Negative current (I_DS) temperature coefficient
- Enhancement mode (normally off)
- DC current gain 10^9
- Matched N-channel and matched P-channel in one package

APPLICATIONS
- Precision current mirrors
- Complementary push-pull linear drives
- Analog switches
- Choppers
- Differential amplifier input stage
- Voltage comparator
- Data converters
- Sample and Hold
- Analog inverter
- Precision matched current sources

ORDERING INFORMATION

<table>
<thead>
<tr>
<th>Package</th>
<th>Operating Temperature Range*</th>
</tr>
</thead>
<tbody>
<tr>
<td>14-Pin</td>
<td>-55°C to +125°C</td>
</tr>
<tr>
<td>CERDIP</td>
<td>0°C to +70°C</td>
</tr>
<tr>
<td>Package</td>
<td>0°C to +70°C</td>
</tr>
</tbody>
</table>

* Contact factory for industrial temperature range.

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### ABSOLUTE MAXIMUM RATINGS

- Drain-source voltage, $V_{DS}$: 13.2V
- Gate-source voltage, $V_{GS}$: 13.2V
- Power dissipation: 500 mW
- Operating temperature range: 0°C to +70°C
- Storage temperature range: -65°C to +150°C
- Lead temperature, 10 seconds: +260°C

### OPERATING ELECTRICAL CHARACTERISTICS

**$T_A = 25°C$ unless otherwise specified**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Symbol</th>
<th>$N$ - Channel</th>
<th>Test Conditions</th>
<th>$P$ - Channel</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gate Threshold Voltage</td>
<td>$V_T$</td>
<td>Min</td>
<td>Typ</td>
<td>Max</td>
<td>Unit</td>
</tr>
<tr>
<td>Offset Voltage $V_{GS1} - V_{GS2}$</td>
<td>$V_{OS}$</td>
<td>10 mV</td>
<td>$I_{DS} = 100\mu A \ V_{GS} = V_{DS}$</td>
<td>10 mV</td>
<td>$I_{DS} = -100\mu A \ V_{GS} = V_{DS}$</td>
</tr>
<tr>
<td>Gate Threshold Temperature Drift</td>
<td>$T_{CVT}$</td>
<td>-1.2 mV/°C</td>
<td>-1.3 mV/°C</td>
<td></td>
<td></td>
</tr>
<tr>
<td>On Drain Current</td>
<td>$I_{DS(ON)}$</td>
<td>25 mA</td>
<td>$V_{GS} = V_{DS} = 5V$</td>
<td>-8 mA</td>
<td>$V_{GS} = V_{DS} = -5V$</td>
</tr>
<tr>
<td>Trans.- conductance</td>
<td>$G_{FS}$</td>
<td>5 mmho</td>
<td>$V_{DS} = 5V \ I_{DS} = 10mA$</td>
<td>2 mmho</td>
<td>$V_{DS} = 5V \ I_{DS} = -10mA$</td>
</tr>
<tr>
<td>Mismatch $\Delta G_{FS}$</td>
<td></td>
<td>0.5 %</td>
<td>0.5 %</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Output Conductance</td>
<td>$G_{OS}$</td>
<td>200 (\mu)ho</td>
<td>$V_{DS} = 5V \ I_{DS} = 10mA$</td>
<td>500 (\mu)ho</td>
<td>$V_{DS} = 5V \ I_{DS} = -10mA$</td>
</tr>
<tr>
<td>Drain Source ON Resistance</td>
<td>$R_{DS(ON)}$</td>
<td>50 (\Omega)</td>
<td>$V_{DS} = 0.1V \ V_{GS} = 5V$</td>
<td>180 (\Omega)</td>
<td>$V_{DS} = -0.1V \ V_{GS} = -5V$</td>
</tr>
<tr>
<td>Drain Source ON Resistance Mismatch</td>
<td>$\Delta R_{DS(ON)}$</td>
<td>0.5 %</td>
<td>$V_{DS} = 0.1V \ V_{GS} = 5V$</td>
<td>0.5 %</td>
<td>$V_{DS} = 0.1V \ V_{GS} = -5V$</td>
</tr>
<tr>
<td>Drain Source Breakdown Voltage</td>
<td>$B_{VDS}$</td>
<td>12 V</td>
<td>$I_{DS} = 10\mu A \ V_{GS} = 0V$</td>
<td>-12 V</td>
<td>$I_{DS} = -10\mu A \ V_{GS} = 0V$</td>
</tr>
<tr>
<td>Off Drain Current</td>
<td>$I_{DS(OFF)}$</td>
<td>0.1 (\mu)A</td>
<td>$V_{DS} = 12V \ I_{DS} = 0V \ T_A = 125°C$</td>
<td>0.1 (\mu)A</td>
<td>$V_{DS} = -12V \ V_{GS} = 0V \ T_A = 125°C$</td>
</tr>
<tr>
<td>Gate Leakage Current</td>
<td>$I_{GS}$</td>
<td>1 (p)A</td>
<td>$V_{DS} = 0V \ V_{GS} = 12V \ T_A = 125°C$</td>
<td>1 (p)A</td>
<td>$V_{DS} = 0V \ V_{GS} = -12V \ T_A = 125°C$</td>
</tr>
<tr>
<td>Input Capacitance</td>
<td>$C_{ISS}$</td>
<td>6 (pF)</td>
<td>6 (pF)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
N-CHANNEL TYPICAL PERFORMANCE CHARACTERISTICS

OUTPUT CHARACTERISTICS

V_{BS} = 0V  
T_A = 25°C  
V_{GS} = 12V

DRAIN-SOURCE CURRENT (mA)

V_{BS} = 0V  
T_A = 25°C  
V_{GS} = 12V

DRAIN-SOURCE VOLTAGE (V)

LOW VOLTAGE OUTPUT CHARACTERISTICS

V_{BS} = 0V  
T_A = 25°C  
V_{GS} = 12V

DRAIN-SOURCE CURRENT (mA)

DRAIN-SOURCE VOLTAGE (mV)

FORWARD TRANSCONDUCTANCE

V_{BS} = 0V  
f = 1kHz  
I_{DS} = 10mA

FORWARD TRANSCONDUCTANCE vs. DRAIN-SOURCE VOLTAGE

DRAIN-SOURCE CURRENT (µA)

V_{BS} = 0V  
T_A = +125°C

TRANSFER CHARACTERISTIC

V_{GS} = V_{DS}  
T_A = 25°C

TRANSFER CHARACTERISTIC WITH SUBSTRATE BIAS

DRAIN-SOURCE CURRENT (µA)

GATE-SOURCE VOLTAGE (V)

R_{DS(ON)} vs. GATE-SOURCE VOLTAGE

V_{DS} = 0.2V  
V_{BS} = 0V

DRAIN-SOURCE ON RESISTANCE (Ω)

GATE SOURCE VOLTAGE (V)

OFF DRAIN - CURRENT vs. TEMPERATURE

V_{DS} = +12V  
V_{GS} = V_{BS} = 0V

OFF - DRAIN SOURCE CURRENT (A)

TEMPERATURE (°C)
TYPICAL APPLICATIONS

CURRENT SOURCE MIRROR

\[
\text{I SOURCE} = \frac{V^+ - V_{t}}{R_{\text{SET}}} \times \text{ISET}
\]

\[
R_{\text{SET}} = \frac{4}{R_{\text{SET}}}
\]

Q1, Q2: N-Channel MOSFET
Q3, Q4: P-Channel MOSFET

CURRENT SOURCE WITH GATE CONTROL

\[
\text{I SOURCE} = \frac{V^+ - V_{t}}{R_{\text{SET}}} \times \text{ISET}
\]

Q1: N-Channel MOSFET
Q3, Q4: P-Channel MOSFET

DIFFERENTIAL AMPLIFIER

\[
V^+ = +5V
\]

Q1, Q2: N-Channel MOSFET
Q3: NMOS Pair
Q4: PMOS Pair

CURRENT SOURCE MULTIPLICATION

\[
\text{I SOURCE} = \text{ISET} \times N
\]

QSET, Q1..QN: ALD 1101 or ALD 1103
Q3, Q4: P-Channel MOSFET
N: Channel MOSFET
TYPICAL APPLICATIONS

BASIC CURRENT SOURCES

N-CHANNEL CURRENT SOURCE

\[
I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - V_t}{R_{\text{SET}}} = \frac{V^+ - 1.0}{R_{\text{SET}}} \approx \frac{4}{R_{\text{SET}}}
\]

Q1, Q2: N-Channel MOSFET

P-CHANNEL CURRENT SOURCE

\[
I_{\text{SOURCE}} = I_{\text{SET}} = \frac{V^+ - 2V_t}{R_{\text{SET}}} \approx \frac{3}{R_{\text{SET}}}
\]

QP1, QP2: P-Channel MOSFET

CASCODE CURRENT SOURCES

Q1, Q2, Q3, Q4: N-Channel MOSFET (ALD1101 or ALD1103)

Q1, Q2, Q3, Q4: P-Channel MOSFET (ALD1102 or ALD1103)