The setup:

The shown photo is an implementation of a voltage divider using CMOS technology in a widely used IC. In this particular CMOS technology, the smallest feature (line width) is about 6 μm. Resistors are implemented using p-doped silicon with p⁺-wells connecting them to the metal contacts.

The challenge:

Estimate the configuration of the divider and the resistance values of its sections.

The winner of February 2019 competition:

Daniel Greisen
Sophomore, BS-EE

The February 2019 Q-MARGIN prize is generous donation by Prof. Donald B. Estreich.