ASYNCHRONOUS COUNTER OPERATION:

The term asynchronous refers to events that do not have a fixed time relationship with each other and, generally, do not occur at the same time. An asynchronous counter is one in which the flip-flops (FF) within the counter do not change states at exactly the same time because they do not have a common clock pulse.

After completing this section, you should be able to:
- Describe the operation of a 2-bit asynchronous binary counter
- Describe the operation of a 3-bit asynchronous binary counter
- Define toggle in relation to counters
- Describe the operation of an asynchronous decade counter
- Develop counter timing diagrams
- Discuss the 74LS93 4-bit asynchronous binary counter

A 2-Bit Asynchronous Binary Counter

Figure 10-1 shows a 2-bit counter connected for asynchronous operation. Notice that the clock (CLK) is applied to the clock input (C1) of only the first flip-flop (FF0), which is always the least significant bit (LSB). The second flip-flop, FF1, is triggered by the Q0 output of FF0. FF0 changes state at the positive-going edge of each clock pulse, but FF1 changes only when triggered by a positive-going transition of the Q0 output of FF0. Because of the inherent propagation delay through a flip-flop, a transition of the input clock pulse (CLK) and a transition of the Q0 output of FF0 can never occur at exactly the same time. Therefore, the two flip-flops are never simultaneously triggered, so the counter operation is asynchronous.

\[ \text{CLK} \rightarrow \text{FF0} \rightarrow \text{FF1} \]

The Timing Diagram: Let's examine the basic operation of the asynchronous counter of Figure 10-1 by applying four clock pulses to FF0 and observing the Q output of each flip-flop. Figure 10-2 illustrates the changes in the state of the flip-flop outputs in response to the clock pulses. Both flip-flops are connected for toggle operation (D = 1, K = 0) and are assumed to be initially RESET (Q = LOW).

\[ \text{CLK} \rightarrow \text{Q0} \rightarrow \text{Q0 (LSB)} \]

The positive-going edge of CLK1 (clock pulse 1) causes the Q0 output of FF0 to be HIGH, as shown in Figure 10-2. At the same time, the Q1 output goes LOW.

\[ \begin{array}{c|c}
\text{CLOCK PULSE} & Q_0 & Q_1 \\
\hline
\text{Initially} & 0 & 0 \\
1 & 1 & 0 \\
2 & 0 & 1 \\
3 & 0 & 1 \\
4 & 1 & 0 \\
5 & 1 & 0 \\
6 & 1 & 0 \\
7 & 1 & 1 \\
8 & 0 & 0 \\
\end{array} \]

Since it goes through a binary sequence, the counter in Figure 10-1 is a binary counter. It actually counts the number of clock pulses up to three, and on the fourth pulse, it recycles to its original state (Q0 = 0, Q1 = 0). The term recycle is commonly applied to counter operation; it refers to the transition of the counter from its final state back to its original state.

A 3-Bit Asynchronous Binary Counter

The state sequence for a 3-bit binary counter is listed in Table 10-2, and a 3-bit asynchronous binary counter is shown in Figure 10-3.A. The basic operation is the same as that of the 2-bit counter except that the 3-bit counter has
eight states, due to its three flip-flops. A timing diagram is shown in Figure 10-3(b) for eight clock pulses. Notice that the counter progresses through a binary count of zero through seven and then recycles to the zero state. This counter can be easily expanded for higher counts, by connecting additional toggle flip-flops.

Propagation Delay. Asynchronous counters are commonly referred to as ripple counters for the following reason. The effect of the input clock pulse is first "felt" by F1. This effect cannot get to F2 immediately because of the propagation delay through F0. Then there is the propagation delay through F5 before F3 can be triggered. Thus, the effect of an input clock pulse "ripples" through the counter, taking some time, due to propagation delays, to reach the last flip-flop.

To illustrate, notice that all three flip-flops in the counter of Figure 10-3 change state on the leading edge of Clk. This ripple effect is shown in Figure 10-4 for the first four clock pulses, with the propagation delays indicated. The LOW->HIGH transition of Q0 occurs one delay time \( t_{PD} \) after the positive-going transition of the clock pulse. The LOW->HIGH transition of Q1 occurs one delay time \( t_{PD} \) after the positive-going transition of Q0. As you can see, F1 is not triggered until two delay times after the positive-going edge of the clock pulse, Clk. Thus, it takes three propagation delay times for the effect of the clock pulse, Clk, to ripple through the counter and change Q0 from LOW to HIGH.

This cumulative delay of an asynchronous counter is a major disadvantage in many applications because it limits the rate at which the counter can be clocked and creates decoding problems. The maximum cumulative delay in a counter must be less than the period of the clock waveform.

**EXAMPLE 10-1**

A 4-bit asynchronous binary counter is shown in Figure 10-5(a). Each flip-flop is negative edge-triggered and has a propagation delay of 10 nanoseconds (ns). Develop a timing diagram showing the \( Q_0 \) output of each flip-flop and determine the total propagation delay time from the triggering edge of a clock pulse until a corresponding change occurs in the state of \( Q_0 \). Also determine the maximum clock frequency at which the counter can be operated.